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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/814,438	03/30/2004	Shoichiro Matsumoto	YKI-0147	5443

23413 7590 08/01/2007

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EXAMINER	
LEWIS, DAVID LEE	

ART UNIT	PAPER NUMBER
2629	

MAIL DATE	DELIVERY MODE
08/01/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/814,438	MATSUMOTO, SHOICHIRO	
	Examiner	Art Unit	
	David L. Lewis	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

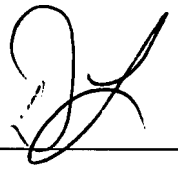
2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *See Continuation Sheet*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.



Continuation of Attachment(s) 3). Information Disclosure Statement(s) (PTO/SB/08), Paper No(s)/Mail Date :3/30/04, 6/17/04, 5/1/06, 5/31/07.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

1. **Claims 1-13 are rejected under 35 U.S.C. 102(e) as being anticipated by Okabe et al. (7154454).**

As in claim 1, Okabe et al. teaches of a light emitting display having an emissive element which emits light in response to a supplied current, **figure 1 or 9, column 2 lines 1-67, column 5 lines 1-67**,

the light emitting display comprising: a drive current generating element for generating a drive current for allowing light to be emitted from the emissive element, **figure 1 item 7**;

a data line onto which a voltage signal and a current signal corresponding to data regarding an amount of light emission from the emissive element are sequentially supplied, **figure 1 item 3**;

and a voltage storage element connected to the data line and for sequentially storing a charge voltage based on the voltage signal and the current signal corresponding to data regarding the amount of light emission, **figure 1 item 6**;

wherein the emissive element emits light based on a drive current generated by the drive current generating element based on the charge voltage stored in the voltage storage element and corresponding to the current signal, **figure 1 item 1, column 5 lines 20-41**.

As in claim 2, Okabe et al. teaches of wherein the voltage storage element is charged based on the voltage signal supplied onto the data line, and the drive current generating element generates the drive current based on the current signal which is supplied following the voltage signal and the voltage storage element is re-charged when the drive current is generated in the drive current generating element, column 2 lines 1-15.

As in claim 3, Okabe et al. teaches of wherein a switch circuit is provided for sequentially switching and supplying the voltage signal and the current signal corresponding to data regarding the amount of light emission onto the data line, figure 1 item 3, said feature inherent as is known.

As in claim 4, Okabe et al. teaches of wherein the drive current generating element is a driver transistor for generating a drive current corresponding to a voltage supplied on its gate, **figure 1 item 7**; the voltage storage element is a

storage capacitor element connected to the gate of the driver transistor for storing the gate voltage, **figure 1 item 6**; a drive current control transistor is provided between the driver transistor and the emissive element for controlling whether or not to supply the drive current from the driver transistor to the emissive element, **figure 1 item 10**; a first write control transistor is connected between the data line and a connection portion between the driver transistor and the drive current control transistor, **figure 1 item 8**; and a second write control transistor is connected between the data line and the gate of the driver transistor, **figure 1 item 4**.

As in claim 5, Okabe et al. teaches of, comprising: switching on the second write control transistor during a period in which the voltage signal is supplied onto the data line to write the voltage signal into the storage capacitor element having one terminal connected to the gate of the driver transistor, **column 2 lines 31-67**; switching on the first write control transistor and the second write control transistor during a period in which the current signal is supplied onto the data line to supply the drive current having a current value equal to that of the current signal to the driver transistor through the first write control transistor, **column 2 lines 31-67,** and, at the same time, to write the gate voltage of the driver transistor when the drive current is supplied into the storage capacitor element; and switching off the first and second write control transistors and switching on the drive current control transistor to supply, through the drive current control transistor to the emissive element, the drive current having a current value equal to that of the current signal written into the storage capacitor element, **column 2 lines 31-67**.

As in claim 6, Okabe et al. teaches of wherein each of a plurality of pixels arranged in a matrix form has such an emissive element, column 1 lines 5-17;

each of a plurality of data lines is provided for pixels in each column of the matrix, column 1 lines 5-17; and pixels of adjacent rows of the matrix are respectively connected to different data lines among the plurality of the data lines, column 1 lines 5-17.

As in claim 7, Okabe et al. teaches of wherein each of the plurality of pixels further comprises the driver transistor, the storage capacitor element, the first and second write control transistors, and the drive current control transistor, figure 1 or 9, column 2 lines 1-67; a selection line for voltage writing and a selection line for current writing are provided for each row of the matrix, figure 1 items 9 and 2; a gate of the second write control transistor is connected to the selection line for voltage writing, figure 1 item 4; and a gate of the first write control transistor is connected to the selection line for current writing, figure 1 item 8.

As in claim 8, Okabe et al. teaches of wherein each of a plurality of pixels arranged in a matrix form has such an emissive element, column 1 lines 5-17; each of a plurality of data lines is provided for pixels in each column of the matrix, column 1 lines 5-17; and pixels of adjacent rows of the matrix are respectively connected to different data lines among the plurality of the data lines, column 1 lines 5-17.

As in claim 9, Okabe et al. teaches of wherein a selection line for voltage writing and a selection line for current writing are provided for each row of the matrix, figure 1 items 9 and 2.

As in claim 10, Okabe et al. teaches of an electroluminescence display circuit, **figure 1 or 9, column 2 lines 1-67, column 5 lines 1-67**,

comprising: a driver transistor for generating a drive current corresponding to a voltage supplied on its gate, **figure 1 item 7**;

an electroluminescence element which is driven by a drive current from the driver transistor, **figure 1 item 1**;

a drive current control transistor connected between the driver transistor and the electroluminescence element for controlling whether or not to supply the drive current from the driver transistor to the electroluminescence element, **figure 1 item 10**;

a first write control transistor having a first region connected to a connection portion between the driver transistor and the drive current control transistor and a second region connected to the data line, **figure 1 item 8**;

a second write control transistor having a first region connected to the data line and a second region connected to the gate of the driver transistor, **figure 1 item 4**;

and a storage capacitor connected to the gate of the driver transistor for storing the gate voltage, wherein a data voltage signal and a data current signal

corresponding to data regarding an amount of light emission are sequentially supplied onto the data line, **figure 1 item 6**;

the second write control transistor is switched on during when the drive current control transistor and the first write control transistor are switched off and a data voltage signal is supplied onto the data line, to write the data voltage signal into the storage capacitor, **figure 1 item 4, column 2 lines 32-67**;

the first write control transistor is switched on during when a data current signal is supplied onto the data line so that the data current signal is supplied to the data line through the driver transistor and the first write control transistor, and, at the same time, a voltage corresponding to the data current signal is written into the storage capacitor via the second write control transistor, **figure 1 item 8, column 2 lines 32-67**;

and the first and second write control transistors are switched off and the drive current control transistor is switched on so that a drive current corresponding to the voltage written into the storage capacitor is generated in the driver transistor and the drive current is supplied to the electroluminescence element via the drive current control transistor and light is emitted, **column 2 lines 32-67**.

As in claim 11, Okabe et al. teaches of an electroluminescence display having an electroluminescence element in each of a plurality of pixels arranged in a matrix form for achieving a display by controlling light emission from each pixel, **column 1 lines 57-67, figure 1 or 9**,

wherein each of a plurality of data lines is provided corresponding to each column of the matrix and a different data line among the plurality of data lines is connected to corresponding pixels for each row of the matrix, **figure 1 item 3**; wherein each adjacent column has a distinct data line to form said matrix display.

and display data is sequentially supplied from the plurality of data lines for pixels of each column of the matrix, **column 1 lines 57-67, figure 1 and 9**, wherein said feature is inherent to said known matrix display having row and column lines to drive the display.

As in claim 12, Okabe et al. teaches of wherein both a data voltage signal and a data current signal regarding display data can be switched and supplied onto each of the plurality of data lines, **figure 1 or 9 items 2 and 9**; and the data voltage signal and data current signal regarding display data are sequentially supplied to each pixel so that the display of each pixel is controlled, **figure 1 item 4, column 2 lines 32-67**.

As in claim 13, Okabe et al. teaches of wherein two control lines are provided for each row of the matrix, **figure 1 item 4, column 2 lines 32-67**; each of the pixels has a plurality of transistors controlled by the two control lines, **figure 1 item 4, column 2 lines 32-67**; and the writing of data voltage signal and the writing of the data current signal into each of the pixels are controlled by the two control lines, **column 2 lines 32-67**.

Conclusion

2. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. **2003/0090446, 6229506, 6930680, 7227517.**

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **David L. Lewis** whose telephone number is **(571) 272-7673**. The examiner can normally be reached on MTWTHF from 8 to 5. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala, can be reached on **(571) 272-7681**. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (571)-273-8300.

4. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Examiner: David L. Lewis
July 9, 2007